# STATEMENT OF INVENTOR

# SIMON KNOWLES

I Simon Knowles, inventor of US Patent Application No. 10/813,628, entitled Apparatus and Method for Control Processing in Dual Path Processor and a person skilled in the art assert that:

Cousin confusingly uses the terms Slot and μSlot interchangeably, and also the terms Instruction and Micro-Instruction interchangeably. This has resulted in the teachings of Cousin being confusing. Below I have tried to clarify what Cousin teaches and how it is different from my invention.

The diagram attached to this note is for the case of GP32 instruction mode (illustrated in Figure 2 of Cousin), without loss of generality. However, from Cousin's description it is clear that the GP16 and VLIW modes have similar restrictions.

It is clear from figure 2 and column 4, lines 32-36 of Cousin ("*According to a second instruction mode, two instructions each having a length of 32 bits are supplied to the decoder...for example W0 and W1 in the cycle 0...*") that in GP32 instruction mode a pair of instructions is passed to the decoder each cycle. This pair of instructions comprises two 32 bit instructions W0 and W1, or W2 and W3 (Instruction0 and Instruction1, or Instruction2 and Instruction3 in my figure) which are decoded by the decoder 8 and sent to the relevant slots (Slot0 or Slot 1). Figure 2 of Cousin also makes it clear that Instruction0 and Instruction1 (W0 and W1) are to be executed together in the same cycle Cycle 0, and Instruction2 and Instruction3 (W2 and W3) are to be executed together in the following cycle Cycle 1. It is not possible, for example, for an Instruction1 and an Instruction2 to be processed together as they are from different instruction pairs executed in different cycles.

Only one of the two 32 bit instructions W0 and W1, or W2 and W3 (Instruction0 and Instruction1, or Instruction2 and Instruction3) can be a control instruction for the general unit. This is apparent when looking at the further steps of the process as explained below.

The two 32 bit instructions Instruction0 and Instruction1 are then processed by the micro instruction generator 10. As illustrated in my figure, the Instruction0 in Slot0 can give rise to a micro-instruction in either or both of the two micro-slots labelled μSlot0, and the Instruction1 in Slot1 can give rise to a micro-instruction in either or both of the two micro-slots labelled μSlot1. The micro-instructions are then sent from the μSlot0 or μSlot1 to a data unit DU1, DU0, an address unit AU1, AU0 or a general unit (a control processing unit).

The Examiner states that since the "macro-instruction" is directed to the general unit, then the general unit must be able to process a plurality of micro-instructions. However, this is not the case. As stated above, a "macro-instruction" is not directed to the general unit, a macro-instruction (being either of the pairs of 32-bit instructions in a 128-bit GP32 Instruction Word) is decoded by the decoder 8 and then processed by the micro instruction generator 10. It is a micro-instruction which is directed to the general unit.

Furthermore, Cousin teaches at column 6, lines 32 to 34 that "*The instructions in the first and second arrays will not both be for the general unit at the same time*" and at column 7, lines 4 to 6 that "*In embodiments of the invention, instructions for the general unit are not provided in both slots at the same time*". This evidently refers to μInstructions occupying the right-hand pair of μSlots in my figure and in figure 1 of Cousin, despite confusing use of the terms "instructions"

and "slots". It is not possible for the left-hand pair of μSlots to contain instructions for the address unit or the general unit . The right-hand pair of μSlots may be used to supply instructions to the address units and the general unit. However, it is not possible for both the right-hand μSlots to contain instructions for the general unit as stated explicitly at column 6, lines 32 to 34 and column 7, lines 4 to 6 of Cousin.

Since it is not possible for both the right-hand μSlots to contain instructions for the general unit, it is not possible for the two Slots (Slot1 and Slot0, between the Decoder 8 and μInstruction Generator 10 of Cousin Figure 1 and my figure) to both contain Instructions destined for the General Unit. This is evident from Cousin's description of the function of the μInstruction Generator 10 and its place in the pipeline (3.32 *et seq*, 4.16 *et seq*), which makes clear that the contents of μSlot0 must come from Slot0 and the contents of μSlot1 must come from Slot1, and that Slot0 and Slot1 are processed in the same cycle (illustrated in Figure 2 of Cousin).

Therefore, since it is not possible for both the Slots to contain instructions for the general unit at the same time, it is not possible for any pair of 32-bit instructions passed to the decoder (which pairing corresponds to an "Instruction Packet" in my application No. 10/813,628) to comprise only instructions for the general unit (only control instructions).

Hence, Cousin does not disclose a decode unit detecting "if the instruction packet define (i) a plurality of control instructions" as claimed in the independent claims of my application No. 10/813,628, since Cousin explicitly states that "*instructions for the general unit are not provided in both slots at the same time*" and consequently, a GP32 Instruction pair (which corresponds to an "Instruction Packet" in my application No. 10/813,628) would not comprise instructions only for the general unit.

Therefore in the processor disclosed by Cousin, instruction pairs such as (W1,W0) in Cousin's Figure. 2 (which correspond to "Instruction Packets" in Application 10/813,628) cannot contain Control Instructions (destined for the General Unit) in both Instruction0 (W0) and Instruction1 (W1) positions, or likewise in both Instruction2 (W2) and Instruction3 (W3) positions. This specifically refers to GP32 mode, but it is evident from Cousin's description that the GP16 and VLIW modes have similar restrictions.

By contrast, my application No.10/813,628 describes any mix of up to 3 Control Instructions in an Instruction Packet (see Figure 2 reference numeral 211 of my application), which is clearly advantageous to simplicity and code density.

I confirm that the facts stated in this statement are within my own knowledge, and that the opinions I have expressed represent my true and complete professional opinion

Simon Knowles

Dated 1 May 2007

## Mapping of "Instruction Words" to "Slots" to "μSlots" to "Execution Units" in Cousin